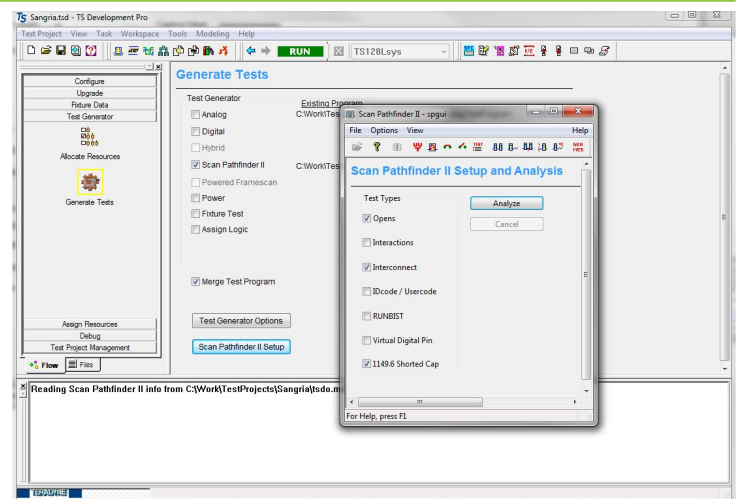


# ScanPathfinder Boundary Scan Option

Boundary Scan Test Generation and Diagnostic Software for TestStation

## KEY FEATURES

- Comprehensive shorts and opens testing for boards with limited test access
- Supports testing boards with a mix of conventional and boundary scan devices
- Effective opens testing for complex 1149.1-compliant digital devices
- Accurate, pin-level diagnostics
- Automatic test generation and diagnostics for boards with single or multiple scan paths
- Integration with TestStation test software
- Rapid execution for high-throughput production testing



Generate and execute 1149.1 compliant boundary scan tests

## Overview

Scan Pathfinder enables Teradyne's production test systems to generate and execute comprehensive tests and diagnostics of IEEE 1149.1 compliant boundary scan boards; even with limited bed-of-nails test access. It provides a complete solution for all of your 1149.1 boundary-scan test requirements on the boards' entire scan path, from opens testing of a single ASIC to thorough shorts and opens testing of a board with a mixture of boundary-scan and conventional-logic devices. Faults are diagnosed to the pin level, enabling you to quickly identify and resolve problems in your manufacturing process.

### Limited Access Problem - Solved

Many high density packaging technologies make the use of bed-of-nails fixtures difficult, if not impossible, and very expensive. Often, to accommodate testability, the board designer must sacrifice component density. Boundary scan minimizes the need for such compromises by providing an electronic bed-of-nails. And with boundary-scan, manufacturers can remove physical access to high density boards without loss of testability and fault coverage.

### Boundary Scan in Production Test

The availability of boundary scan has not changed the goals of production test:

1. Detection and diagnosis of shorts between nodes
2. Verification that correct components are soldered to the board and there are no opens
3. Verification that components were not damaged during the assembly process.

Boundary scan provides a way to achieve these goals, even if access is limited and components are complex. And semiconductor manufacturers have responded to the call for boundary scan by embedding standard test circuitry into a growing number of microprocessors, support components, and

Programmable Logic Devices. However, today's printed circuit board typically employs both boundary-scan and conventional devices. Although partial use of boundary-scan at the board level produces better fault coverage of device opens, it also creates a new challenge to detect and diagnose shorts between un-nailed boundary-scan nodes and nailed conventional nodes. Teradyne's Scan Pathfinder provides the tools that enable you to use boundary scan to its maximum advantage today, to solve production test challenges for your entire board, regardless of its configuration and boundary scan mix.

### Solving Boundary Scan Testing Challenges

Scan Pathfinder helps solve the two most pressing challenges of boundary scan. The first is the problem of the length of time and its associated costs that are required to develop comprehensive test programs for ASICs. The second is maintaining high fault coverage for boards that have a mix of boundary scan and conventional devices.

Teradyne's Scan Pathfinder solves the time and cost problems of test generation for ASICs by supplementing in-circuit techniques to greatly reduce the number of complex test vectors required to perform comprehensive tests for shorts and opens. For boundary-scan ASICs with full access, digital tests for process faults can be generated in a matter of minutes. For boundary-scan ASICs without full access Scan Pathfinder uses descriptive models written in the industry standard Boundary Scan Descriptive Language (BSDL). Since there is no need to learn device functionality, programming time is greatly reduced. Many BSDL models are

available from Teradyne and device manufacturers for commercially available ICs. Teradyne also offers BasicSCAN software which assists users of ASICs in developing their own BSDL models.

The second, more complex, yet very common challenge is testing boards comprised of a mixture of conventional and boundary-scan devices without full physical access. On boards of this type the challenge of detecting shorts, which represent the largest proportion of potential faults, is compounded by the lack of bed-of-nails access to a potentially large percentage of the board. Because of this, it is imperative that the test tools are able to perform an interactions test to detect the shorts between the nodes with bed-of-nails access and the boundary-scan nodes without access. Without the interactions test, executing a boundary-scan interconnect tests can lead to unpredictable results and misdiagnosis. With the successful execution of the interactions test, you have eliminated all possible sources of confusion or ambiguity in the boundary-scan interconnect test.

Scan Pathfinder is the only boundary-scan test-generation and diagnostic toolset to provide the patented interactions test capability, making it the only total solution for production test of limited access, partial boundary-scan boards. The boundary-scan tests are generated automatically for the entire board whether the design contains single or multiple independent scan paths, or multiple scan paths that share a common TDI and TDO signal, or any configuration that employs a combination of these schemes.

Scan Pathfinder is integrated with Teradyne's world-class automatic test generation (ATG) software and provides the highest fault coverage and diagnostic resolution of any system available.

The tests generated operate the entire scan path as one unit and provide full interconnect testing. This includes opens and shorts, plus verification that the testability circuitry is operable with multiple faults being detected and accurately diagnosed to the pin level in a single execution of the test program.

## Ensuring Diagnostic Accuracy

Scan Pathfinder gives you the highest diagnostic accuracy, eliminating unnecessary rework on good boards and minimizing repair time on faulty boards. And with many manufacturers recommending only one repair action for complex devices, you can't afford to misdiagnose a problem.

Scan Pathfinder places a unique ID on all boundary scan nodes. If a test fails, Scan Pathfinder can find the source of the faults by comparing the expected node ID with the sensed node ID. If necessary, the diagnostics will run additional "adaptive" patterns to clarify ambiguous nodes and ensure that faults are accurately identified. Scan

Pathfinder delivers the diagnostic capability to identify the specific set of nodes where an open or short exists. This provides the accurate and detailed information you need to keep your manufacturing process under control.

## Putting Scan Pathfinder to Work

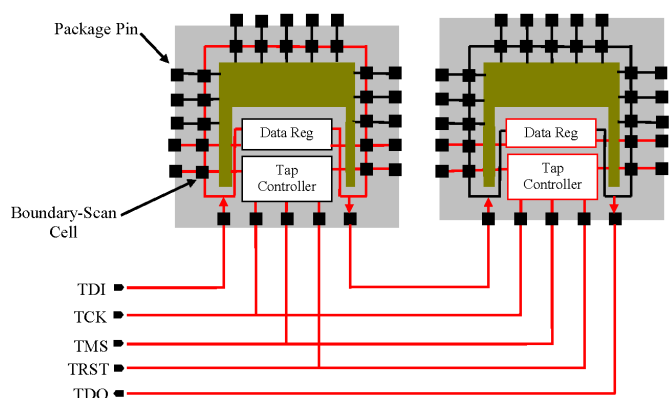
To take full advantage of the benefits offered by boundary scan, Teradyne makes Scan Pathfinder available as an option for every system in the TestStation Family of In-Circuit Test Systems. This permits a sharing of resources and capabilities, which greatly enhances the test development process while relieving much of the programming burden. Furthermore, the integration of conventional and boundary-scan tools ensure optimum solutions for fast test execution of the entire printed circuit board. And this is all accomplished without any additional hardware requirements.

## Generating User-Selectable Tables

### Scan-Path Integrity Test

The Scan-Path Integrity Test verifies that Test Access Ports (TAPs) on the entire scan path are operational and the TAP signals can be driven by the tester resources. This test also verifies a test pattern can be shifted through the Instruction Register and the two mandatory data registers, Bypass and Boundary Scan. If the device supports the IDCODE instruction it will be tested to ensure the correct device has been placed.

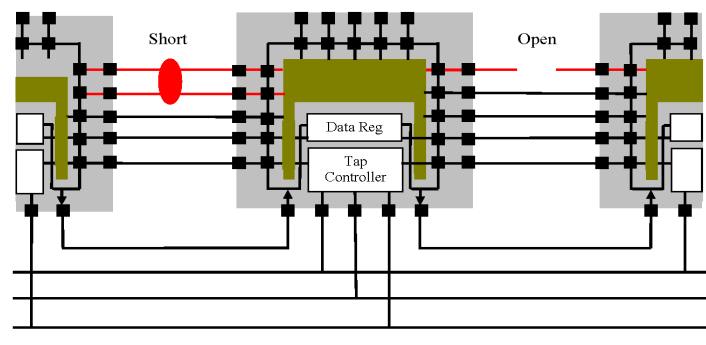
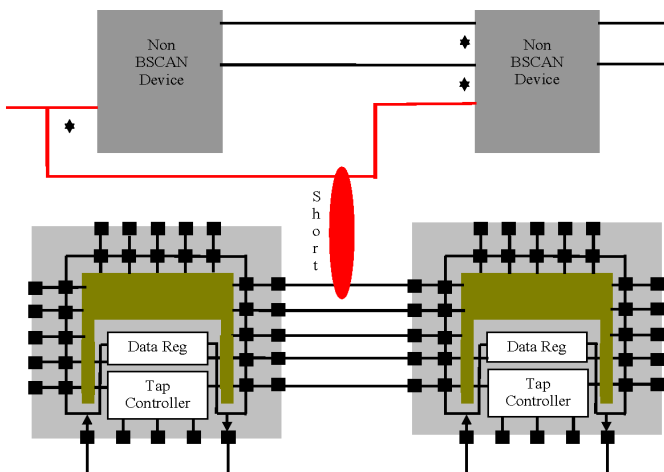
The Scan-Path Integrity Test diagnostics are capable of reporting open or stuck TAP signals, bad scan paths, and wrong Instruction Register capture values. The diagnostics can also identify and report multiple device failures on the same path. The diagnostic report includes failing node, pin, and device information. On boards with multiple scan paths, diagnostics can identify shorts between TDI/TDO of these paths, even when these nodes are not nailed.



## Interactions Test

The Interactions Test detects shorts between nailed conventional nodes and unnailed boundary-scan nodes.

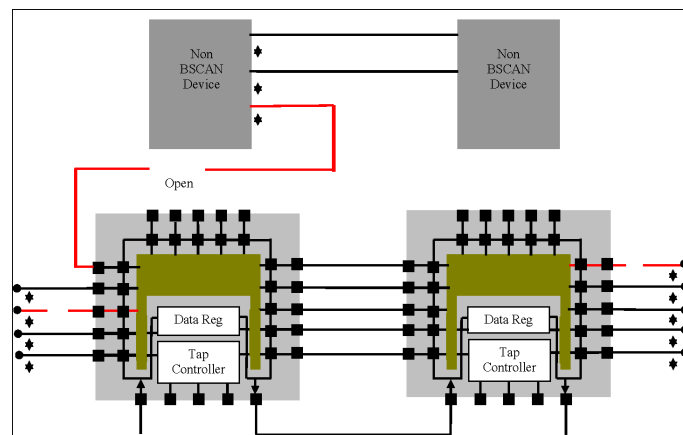
The Interactions Test diagnostics reports any shorts between boundary-scan and non-boundary-scan nodes. The report is capable of listing multiple failures and includes node, pin, and device information.



## Boundary-Scan Opens Test

The Opens Test verifies opens between tester driver/sensors and boundary-scan input and boundary-scan output nodes.

The Boundary-Scan Opens Test diagnoses opens to the component pin. In addition, multiple opens on the same node, as well as multiple opens pins on the same component, are diagnosed accurately.



## Interconnect Test

Interconnect Test detects shorts and opens between unnailed boundary-scan nodes

*The end result of these tests is fault coverage for shorts and opens affecting the scan path...shorts between inaccessible boundary-scan nodes...shorts between inaccessible boundary-scan nodes and accessible conventional nodes...and open input and outputs on boundary-scan devices.*

### Test Capabilities:

Test	Fault Detected	Benefit
Hardware Integrity	<ul style="list-style-type: none"> <li>- Shorts and opens on the boundary scan path TDI/TDO shorts among multiple scan paths</li> <li>- Incorrect part</li> </ul>	<ul style="list-style-type: none"> <li>- Prevent false device diagnostics due to TAP failure, or shorts between control lines when multiple scan paths are present</li> </ul>
Boundary Scan Opens	<ul style="list-style-type: none"> <li>- Opens between nailed nodes and boundary scan inputs and outputs</li> </ul>	<ul style="list-style-type: none"> <li>- Find opens caused by a variety of defects</li> <li>- Accurately diagnoses multiple opens per node and multiple open pins per boundary scan component</li> </ul>
Interconnect	<ul style="list-style-type: none"> <li>- Shorts and opens on unnailed boundary scan nodes and edge-connector nodes</li> </ul>	<ul style="list-style-type: none"> <li>- Allows testing on nodes without bed-of-nails access</li> </ul>
Interactions	<ul style="list-style-type: none"> <li>- Shorts between pure boundary scan nodes and nailed conventional nodes</li> </ul>	<ul style="list-style-type: none"> <li>- Addresses the larger proportion of total potential faults involving boundary scan components</li> </ul>