Teradyne ICT Application Brief	Teradyne, Inc www.teradyne.com	Author: Charles Robinson Published Date: October 2011

Migrating JTAG Technologies Boundary Scan Tests to Test Station Hardware

Using Symphony TS / DSM tool to convert native JTAG Boundary Scan tests to Test Station test language eliminates the need for 3rd party hardware.

Application Overview

JTAG Technologies ProVision is a popular JTAG test development and execution tool used to test for basic shorts/opens/bad/missing defects and to perform memory and cluster tests, and in-system programming of memory and CPLDs on circuit boards. ProVision tests are often developed during the engineering and prototype phases of board development and TestStation users would often like to be able to reuse these applications when moving to TestStation for production test.

The JTAG Technologies Symphony TS/DSM tool allows one to take a JTAG Technologies ProVision PC based test set and to migrate it to the Test Station ICT system. The resulting test set can be run on the Test Station system without the need for any 3rd party hardware in the system or fixture. Please note that the Symphony TS/DSM tools are also compatible with the JTAG Technologies Classic software.

Please note that ProVision in-system programming applications for Flash memory and CPLDs cannot be converted using Symphony TS/DSM. These ProVision applications can be supported on the TestStation using the Symphony TS/CFM product, which uses JTAG Technologies hardware and software to execute these applications. For additional information on the Symphony TS/CFM product please see the Teradyne ICT Application Brief called "**Utilizing JTAG Symphony_CFM on TestStation**".

Hardware Requirements

The Symphony TS/DSM tool uses the Test Station digital subsystem for driving and sensing the boundary scan Test Access Port (TAP) signals TDI, TDO, TMS and TRST. The TCK signal is driven by a tester Clock Driver. The boundary scan vector data is stored in the Deep Serial Memory.

A dual-stage fixture is considered best practice when fixturing a UUT for 3rd party boundary scan test at ICT. A dual-stage fixture allows for two levels of nail contact to the UUT. When performing standard in-circuit tests, the full bed-of-nails will be in contact with the UUT. During

the boundary scan test, a minimum set of nails will contact the UUT, typically power, ground, TAP and control. This provides better signal integrity for the boundary scan tests by removing the loading effects presented by the full bed-of-nails.

Summary:

- System must contain digital resources (IE no analog only systems)
- System must have CST license to enable Clock Driver pins
- System must have a Deep Serial Memory option
- Dual-stage fixture for UUT

Software Requirements

No special Teradyne software is required to run the Symphony TS/DSM tool. However several JTAG Technologies software modules are required, both to perform the test conversion and to provide the Boundary Scan test diagnostics. These modules are:

- JTAG to Teradyne test vector conversion software
- Result Collector software
- Software Control module for result collector & diagnostics
- Node locked boundary-scan diagnostics (BSD) software

These modules are contained within the Symphony TS/DSM package, Teradyne PN 613-915-01.

Application Examples

The migration is a two step process where the existing JTAG Technologies ProVision tests are first converted into Test Station test language and then the converted tests are integrated into the main Test Station test program.

The user will first need to create or obtain a passing JTAG Technologies ProVision test project for the target UUT. A ProVision test project consists of individual tests called “applications”. Each application will have its own folder located in the ProVision project. All the files related to an application will reside in this folder.

For the Symphony conversion, two files will be used from each application folder, the GEN and APL file. Each file will be named uniquely for the application folder that it is located in, so the INTER application, the files would be named “INTER.GEN” and “INTER.APL”. The user will create a folder where the conversion will be done and copy into this folder all the GEN and APL files for the applications to be converted. The user will open a DOS window and point to this folder, where he will run the Symphony conversion tool on each application file set. The result of each conversion will be a unique Test Program (TPG) and Deep Serial Data file (DDS) for each application.

These unique TPGs will typically be integrated into a larger ICT program. This will consist of moving common elements like variable, subroutine and clock declarations into their appropriate locations and then either calling the test code, say using a #INLCUDE statement, or cutting and pasting the test code into the main program or subroutines.

Code used to start and stop the JTAG diagnostic routine must be moved to LOAD and UNLOAD subroutines. There will also be code where the JTAG diagnostic routine will be

called for failing tests and where the JTAG diagnostics will be redirected to the standard Test Station message output. This should all be integrated into a common location in the main test program.

Additional work may be done to customize the test flow based on the pass/fail conditions of various tests, to add additional diagnostic messages or to otherwise enhance the overall integration.

Additional Information

For additional information on Symphony TS/DSM and Symphony TS/CFM products, please refer to the "Symphony FAQ" which may be obtained from the Teradyne website at www.teradyne.com or from your Teradyne representative.

Application information on the Symphony TS/CFM product may be found in the Teradyne ICT Application Brief called "**Utilizing JTAG Symphony_CFM on TestStation**".